

# Modeling the Impact of Power/Ground Via Arrays on Power Delivery

Jason R. Miller and Istvan Novak  
Sun Microsystems, Burlington, MA  
e-mail: jason.r.miller@sun.com, istvan.novak@sun.com

## Abstract

*The impact of via arrays on power and ground planes is examined in this paper. Measurements of the plane impedance were made on a 8 x 8 via array as a function of via pair location. The results from full-wave field solution are compared to measurement data and excellent correlation is obtained. The results show that the impedance and effective inductance is a strong function of location within the array. The lowest impedance and inductance is measured on the array perimeter. A 4 X increase in the impedance and inductance occurs at the array center. By parameterizing the antipad diameter in simulation it is found that the impedance increases sharply when the antipads overlap.*

## Introduction

Multi-layered high-performance packages, such as a ball-grid-array (BGA) packages, increasingly look to improve current supply capabilities by including additional power/ground vias. These vias are used to provide a low-inductance connection between the printed circuit board (PCB) and the die. However, increasing the number of power/ground vias sacrifices the power/ground plane area under the chip because of antipad cutouts. Thus, the denser the power/ground via field, the less plane remains to provide a stable power supply. It has been shown that the effective inductance of a plane pair increases with the density of the via array [1]. On the other extreme, reducing the via density in an effort to preserve the solidity of the power/ground plane pair could result in unacceptable voltage supply fluctuation. Another consideration is that the distribution of PCB plane metal is not uniform; the vias on the perimeter of the via field benefit from a more solid power/ground plane pair whereas the vias in the center of the field can be contacting a plane perforated to such an extent that only localized islands of metals exist. In a prior work, Yang et al. found that the antipad array can have a significant impact on the plane impedance and plane resonances, but did not examine the spatial dependence of the impedance, i.e. the impedance as a function of the via pair location within the array [2]. The impact of antipad size on the impedance was also not considered. In this work, the plane impedance of an 8 x 8 via array is measured as a function of via pair location. These data are then compared to the results from a full-wave field solver using HFSS [3]. Finally, the antipad diameter is parameterized to examine the impact of antipad overlap on the impedance and equivalent inductance.

## Test Board Measurements

To evaluate the impact of via array effects, a number of test structures and boards were designed and fabricated. The test board discussed here consisted of a 8 x 8 via array of alternating power/ground vias centered on a 2.5" square plane pair with an 8 $\mu$ m thick dielectric. Figures 1 and 2 show the staggered arrangement of the power/ground via pairs and a cross-section of the structure. Each via pair can be uniquely identified using the row and column identifiers shown in Figure 1. For example, (A1,B1) corresponds to the via pair located in the bottom left hand corner. The matrix is fully symmetric; thus, (A1,B1) has the same geometry and environment as (G8,H8). The antipad diameter and via center-to-center distance are 58 mils and 50 mils, respectively. The via diameter is 22 mils and the plated through holes (PTH) have a wall thickness of about 1.3 mils.

An HP 4396B vector network analyzer (VNA) was used to measure the self-impedance magnitude and phase from 100 kHz to 1.8 GHz. With the board secured on its side, semirigid coaxial probes were used to contact the via pairs from opposite sides of the board. A full-two port calibration was performed. The power/ground via pairs were then measured as a function of pair location. Real and imaginary  $S_{21}$  measurement data were processed and the corrected self-impedance magnitude and phase was obtained [4].

Figure 3 plots the impedance measured on the diagonal of the matrix from the corner (A1,B1) to the center (D4,E4). Also shown for reference is the measured impedance at a stand-alone via pair, outside of the array. Up to about 10 MHz the locations show similar self-impedance profiles as the impedance is dominated by the static capacitance of the plane pair. Above 10 MHz, the impedance profiles diverge significantly; the plane perforation pushes the series resonance lower and increases the plane equivalent inductance. The largest impedance change within the array is observed one step in from the corner location. Thereafter, the impedance changes are smaller. In fact, the final two

measurement pairs near to the center are overlapping on this scale. Figure 4 plots the measured equivalent inductance ( $L = \text{Im}\{Z\}/\omega$ ) at the via pairs moving diagonally from the corner via pair to the center of the array. The measured equivalent inductance at the stand-alone via pair is shown as reference. The inductance is found to be a strong function of location within the array. Figure 5 plots the ratio of the equivalent inductances at the via pairs, measured along the diagonal, to the inductance at the stand-alone via pair. The equivalent inductance within the array is found to vary by as much as 4 X. By measuring rows AB, BC, CD, DE across each column (1-8) and taking advantage of the symmetry of the structure, it is possible to obtain a plot of the impedance and inductance of the entire array. Figures 6 and 7 plot the impedance and equivalent inductance of the array at 1 GHz, respectively. Moving in from the array perimeter, the impedance magnitude and equivalent inductance are found to increase sharply towards the array center.

## Simulation Results

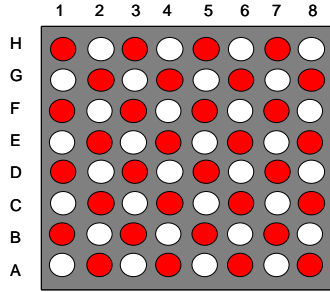
Ansoft HFSS [3], a 3D full-wave field simulator, was used to extract the S-parameters of the entire via array. Lumped gap ports of 50 ohms were defined at each of the via pad pairs, on the top and bottom of the test board, and the two-port S-parameters were calculated for each pair. An absorbing boundary was used to simulate the open nature of the problem. In order to properly capture the antipad overlap, the antipad was modeled with 24 facets, very closely approximating the true area overlap. By meshing both internally and on the surface of the metal it was found that meshing the surface was sufficient to capture the impedance above 100 MHz. Real and imaginary  $S_{21}$  solver data was then processed and the corrected impedance magnitude and phase information was obtained using the same procedure as above. Figures 8 and 9 compare the impedance measured and simulated at the corner and center of the array (A1,B1) and (D4,E4), respectively. Overall, excellent agreement is obtained between the measurement and simulation. The resonance at about 170 MHz, more pronounced in the corner of the array, was not captured by the simulation and remains to be understood. By parameterizing the antipad diameter in the field solver, it was possible to examine the impact of antipad overlap on the impedance and equivalent inductance as a function of location within the array. Figure 10 plots the equivalent inductance of the locations (A1,B1) and (D4,E4) as a function of antipad overlap. In this geometry, an antipad overlap of zero means that the antipad diameter is 50 mils. For the two pair locations the inductance at 500 MHz and 750 MHz was compared. Both the 500 MHz and 750 MHz plots show that the inductance at the two locations increases sharply when the antipad overlap is positive. A positive value for the antipad overlap implies that the via center-to-center spacing is such that there is an overlapping opening in the power and ground planes. Figure 11 shows the same graph as Figure 12, except on a log-linear scale. This graph more clearly shows that in the case of negative overlap, the inductance does increase as the antipad diameter increases although not as sharply. Figure 12 plots the ratio of the inductance at (D4,E4) over the inductance at (A1,B1), at 500 MHz and 750 MHz. The plot shows that with positive antipad overlap the center via pair locations will have much higher inductance than the perimeter vias. Conversely, with negative antipad overlap, the ratio of the inductances of the center vias to the perimeters vias asymptotically approaches one.

## Conclusions

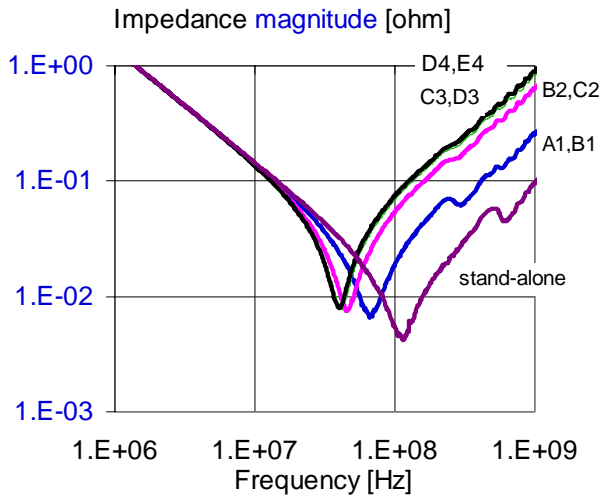
Measured and simulated data on via arrays showed that plane perforation can increase the impedance and inductance of via pairs within the array. Very good correlation was obtained between measurement and simulated data. The impedance in the array was found to be spatially dependent. In the test board geometry used here this variation was as high as 4 X. By simulating other antipad configurations it was shown that this variation is a strong function of antipad overlap. These results indicate that antipads in power/ground via arrays should not overlap in order to reduce the impedance and maintain a more uniform impedance across the array.

## References

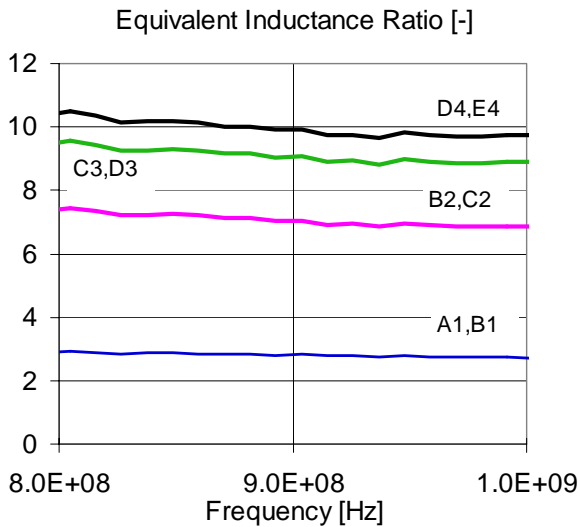
1. Hyungsoo Kim, Jinguok Kim, Youchul Jeong, Jongbae Park and Joungho Kim, *Analysis of Via Distributions Effect on Multi-layered Power/Ground Transfer Impedance of High Performance Packages*, Proceedings of the 11th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 171-178, Oct. 2002.
2. Zhiping Yang, Jim Zhao, Sergio Camerlino, and Jiayuan Fang, *Impact and Modeling of Anti-Pads on Power Delivery System*, Proceedings of the 12th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 117-120, Oct. 2003.
3. Ansoft HFSS Version 9.2.1, from Ansoft Corporation.
4. Istvan Novak, *Measuring MilliOhms and PicoHenrys in Power Distribution Networks*, DesignCon2000, Feb. 2000.



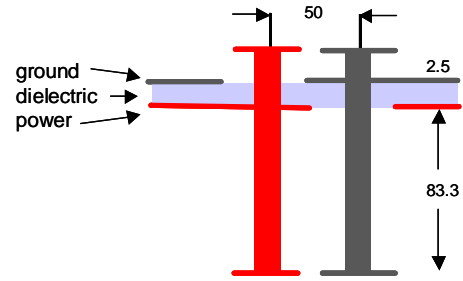
**Fig. 1:** Via matrix arrangement. The white filled circles are ground vias. The array is centered on a 2.5" square plane pair.



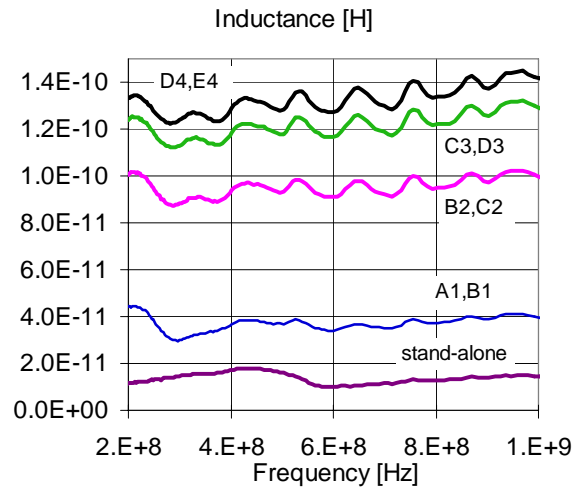
**Fig. 3:** Measured impedance profiles at via pairs on the diagonal starting with (A1,B1) progressively moving towards the center (D4,E4). A stand-alone via pair is also shown as reference.



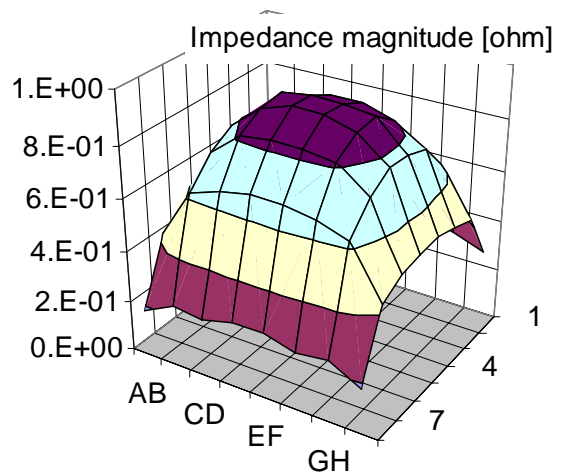
**Fig. 5:** Ratio of the equivalent inductance at via pairs along the diagonal of the array relative to the stand-alone via pair.



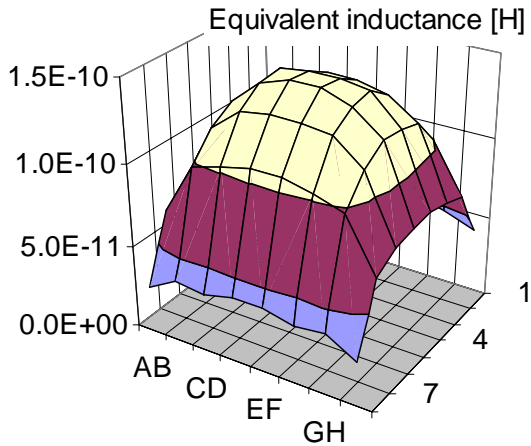
**Fig. 2:** Test board geometry with nominal thickness shown. Units are in mils unless otherwise noted. The dielectric thickness is 8  $\mu$ m, copper weight is 1 oz.



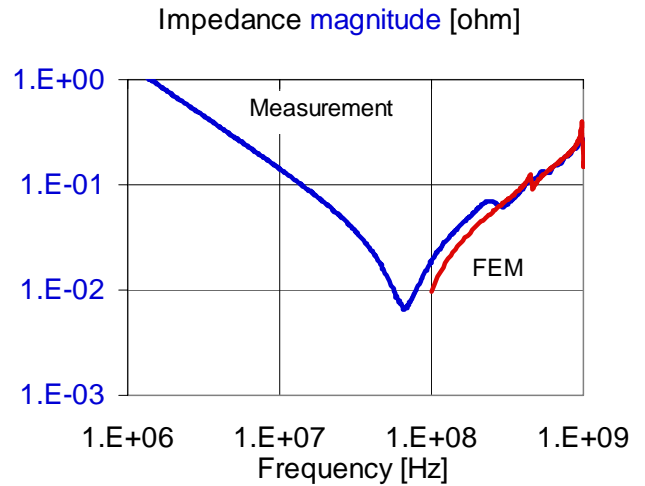
**Fig. 4:** Measured equivalent inductance at via pairs on the diagonal starting with (A1,B1) progressively moving towards the center (D4, E4). A stand-alone via pair is also shown as reference.



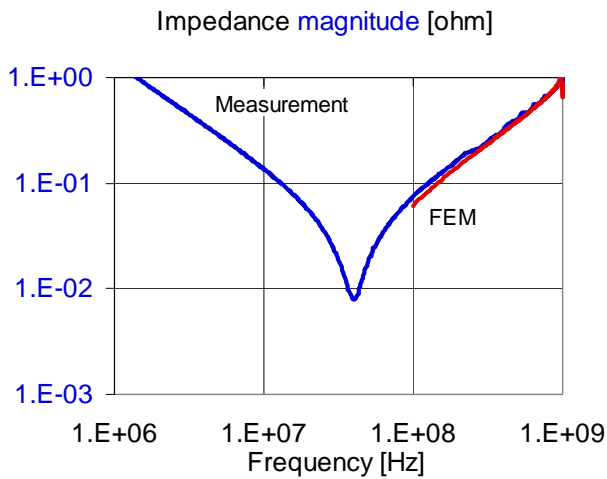
**Fig. 6:** Plot of measured impedance magnitude of the entire array at 1 GHz.



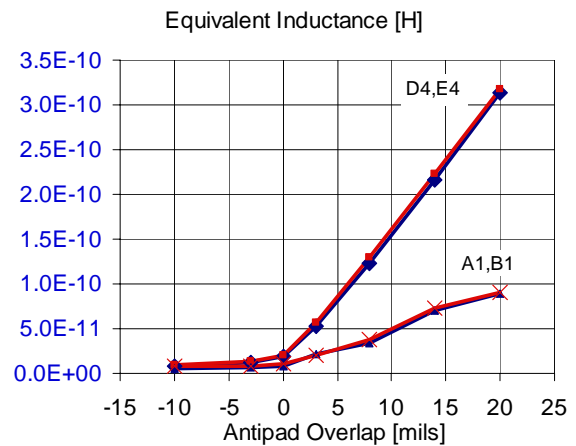
**Fig. 7:** Plot of the equivalent inductance of the entire array at 1 GHz.



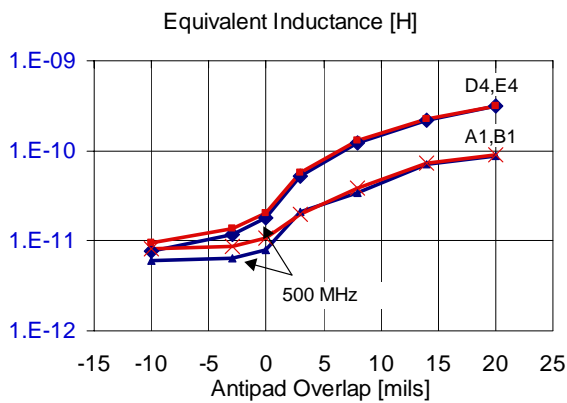
**Fig. 8:** Measured and simulated impedance data at a via pair located at the corner of the array (A1,B1).



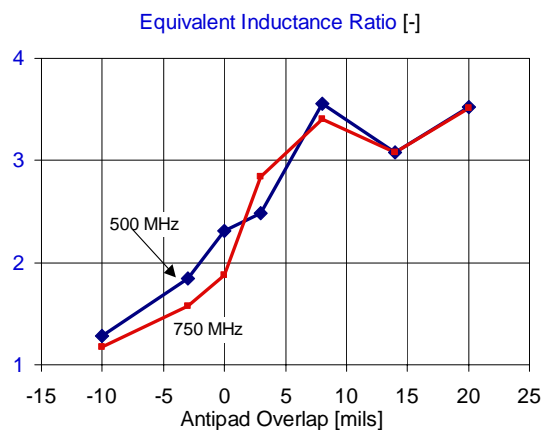
**Fig. 9:** Measured and simulated impedance data at a via pair located at the center of the array (D4,E4).



**Fig. 10:** Simulated equivalent inductance at the corner via pair (A1,B1) and (D4,E4) as a function of the antipad overlap.



**Fig. 11:** Simulated equivalent inductance at the corner via pair (A1,B1) and (D4,E4) as a function of the antipad overlap on a log-linear scale.



**Fig. 12:** Ratio of the inductance at (D4,E4) to (A1,B1) at 500 MHz and 750 MHz as a function of antipad overlap.