



# Impedance of High-Speed Traces: Specification and Consistency in Manufacturing

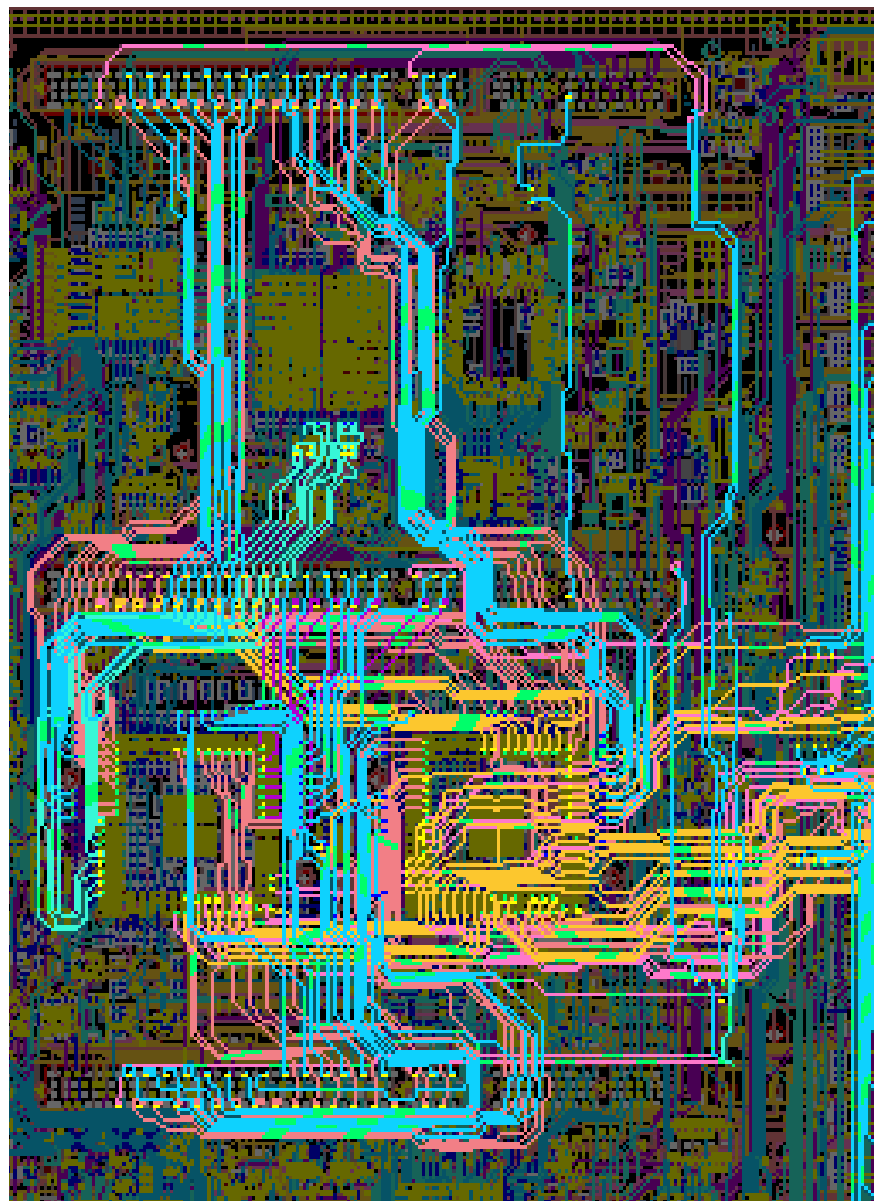
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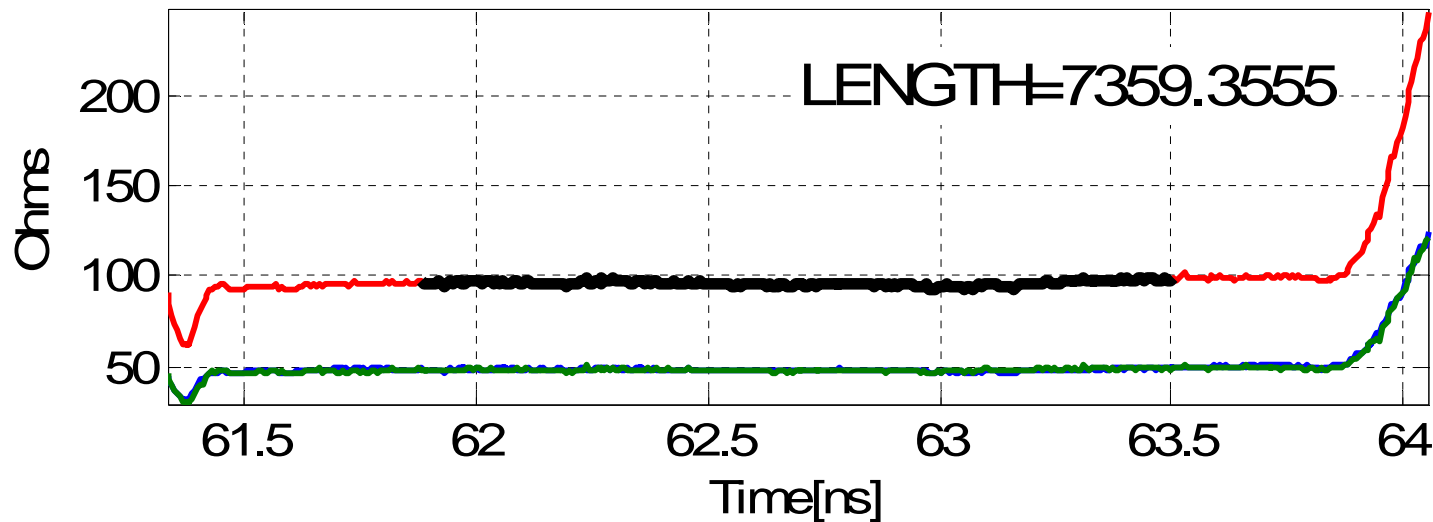
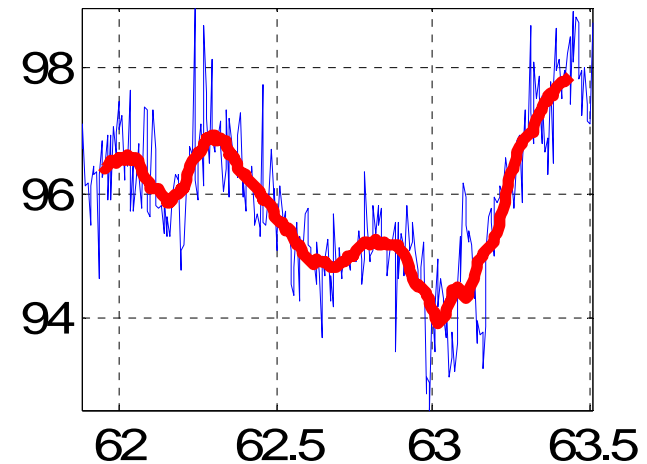
# The DUT

- 20-layer
- 10"x15" outline
- Many Gbps lanes
- Two separate fabricators (A and B)

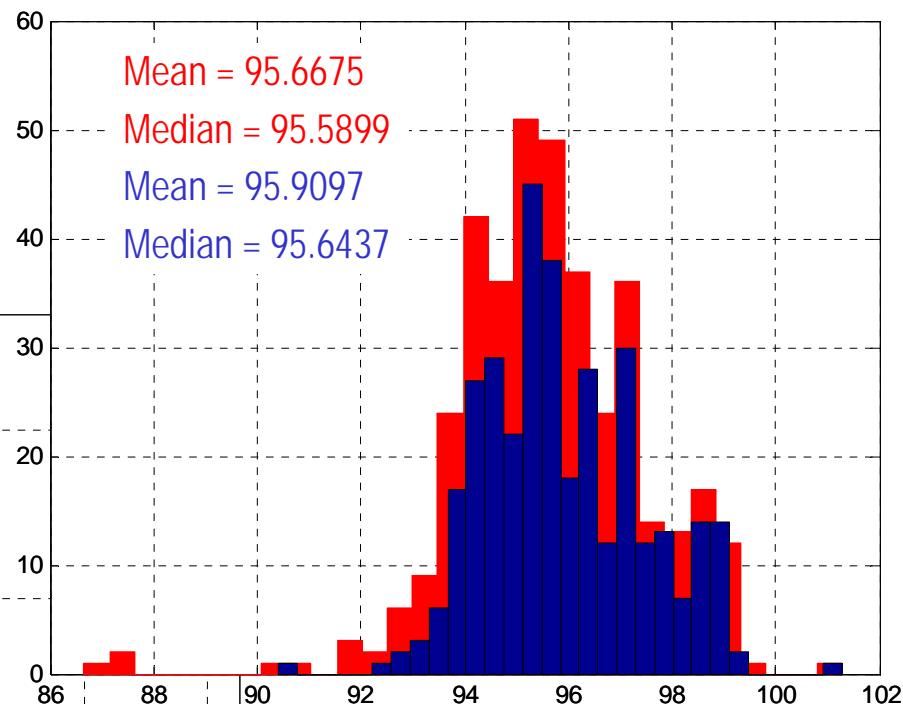
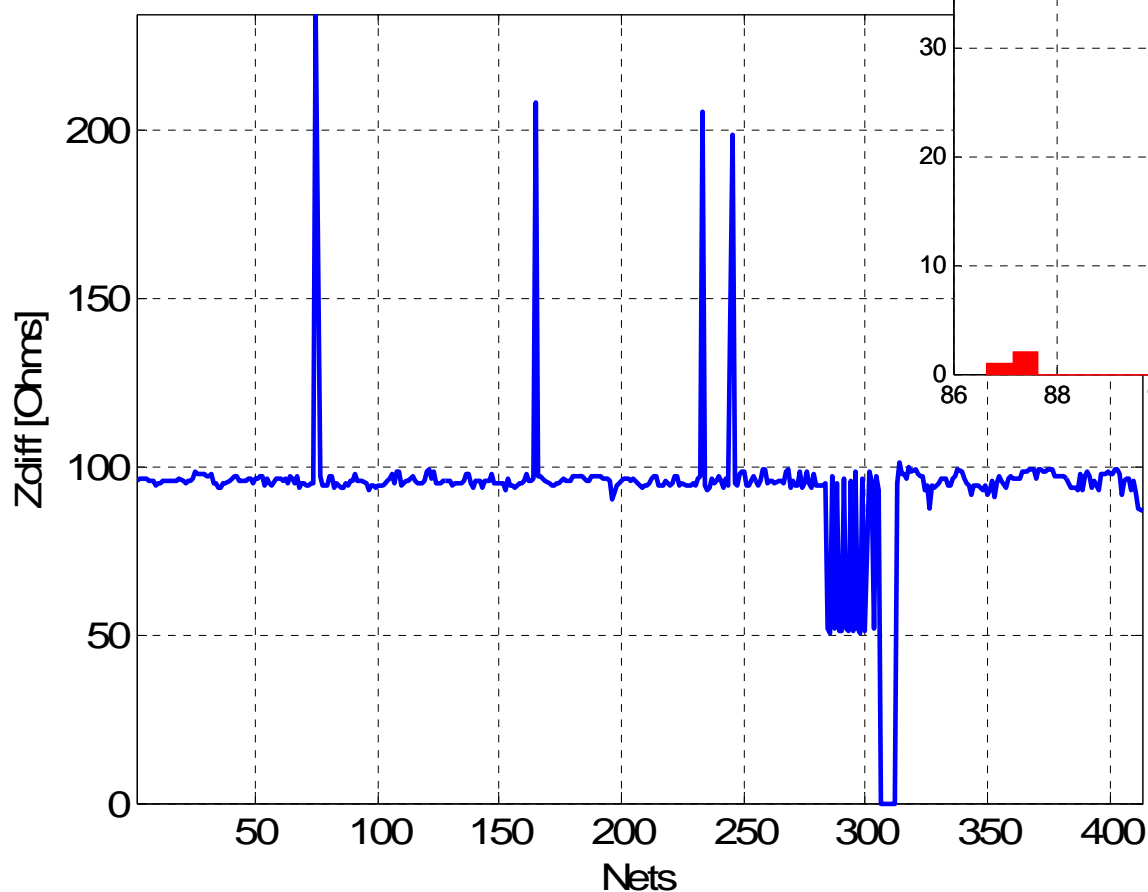


# The Test Procedure

- DM and CM impedances measured
- Via launch and trace-end excluded
- Impedances are plotted per net

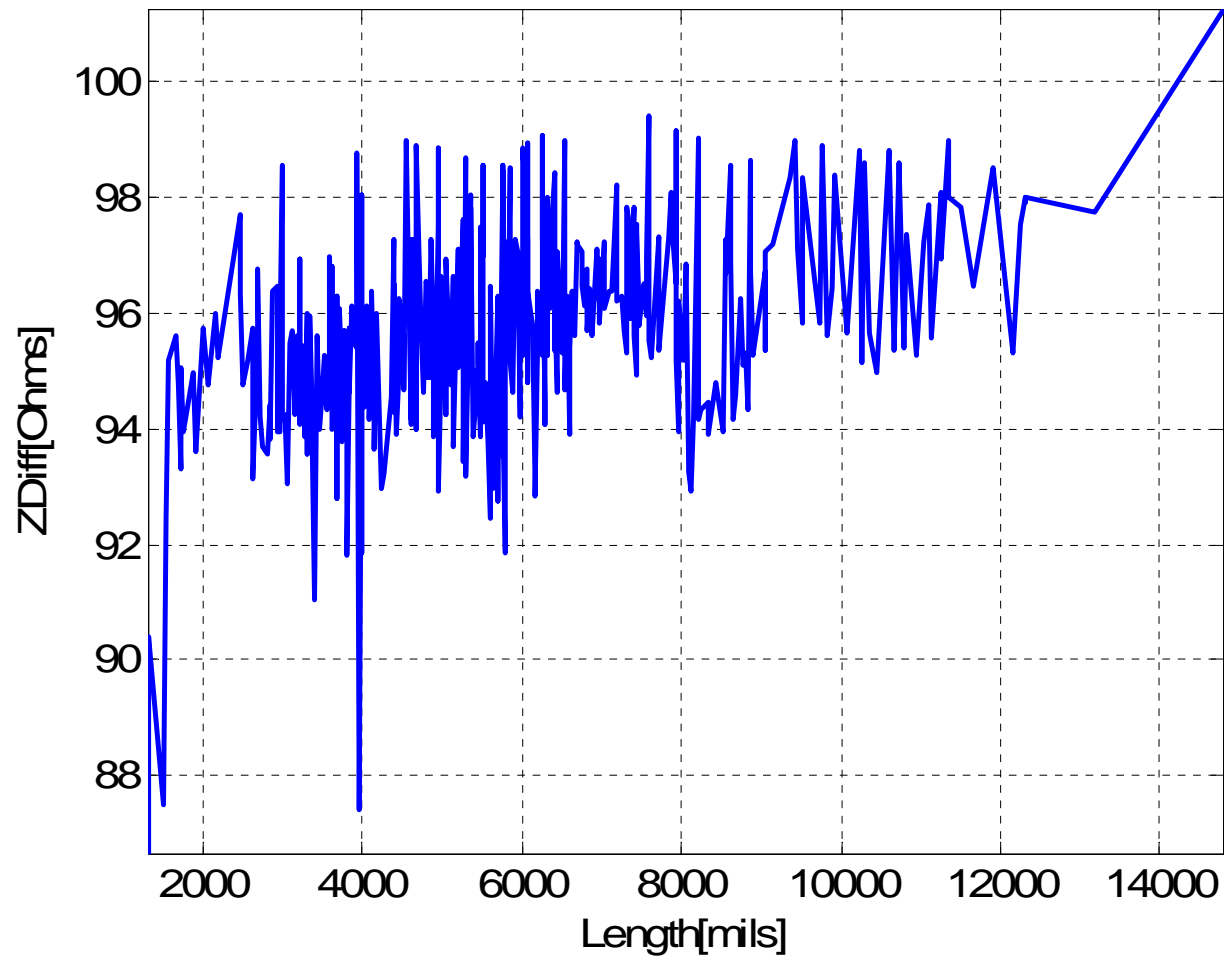


# Statistics Fab. A



- Consistent impedance  
Some outliers:
- Measurement errors
  - Extra vias on net

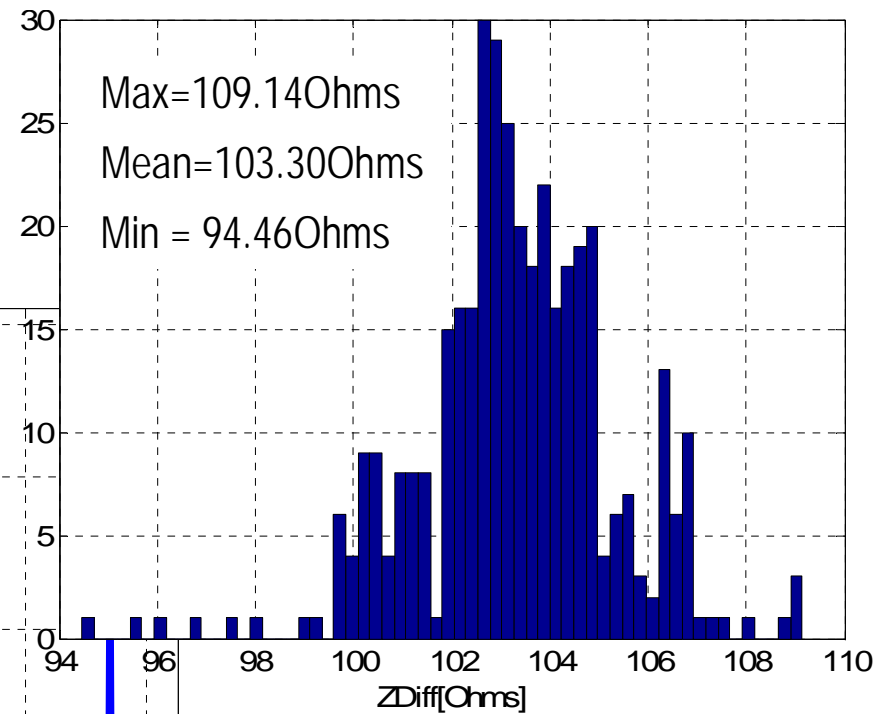
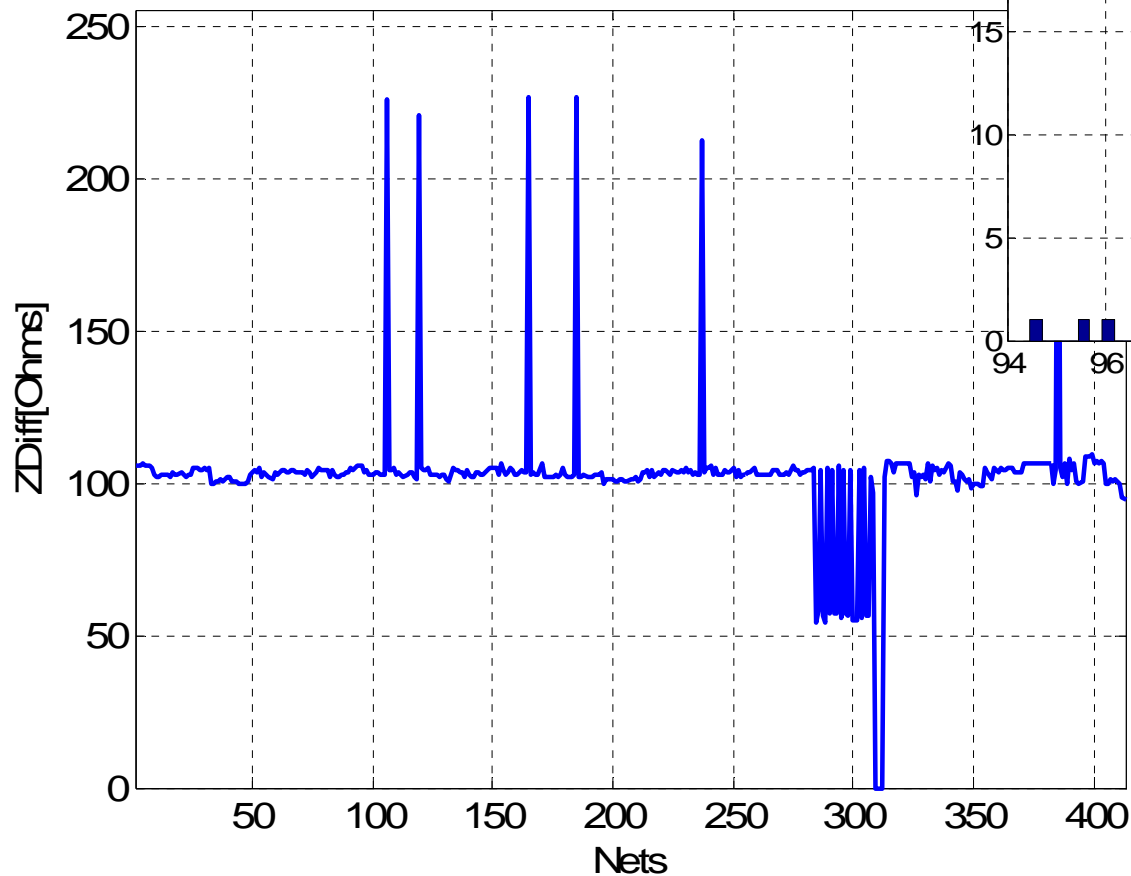
# Measured Differential Impedance vs. Trace Length (Fab. A)



On lossy traces,  
measured impedances  
rises with time

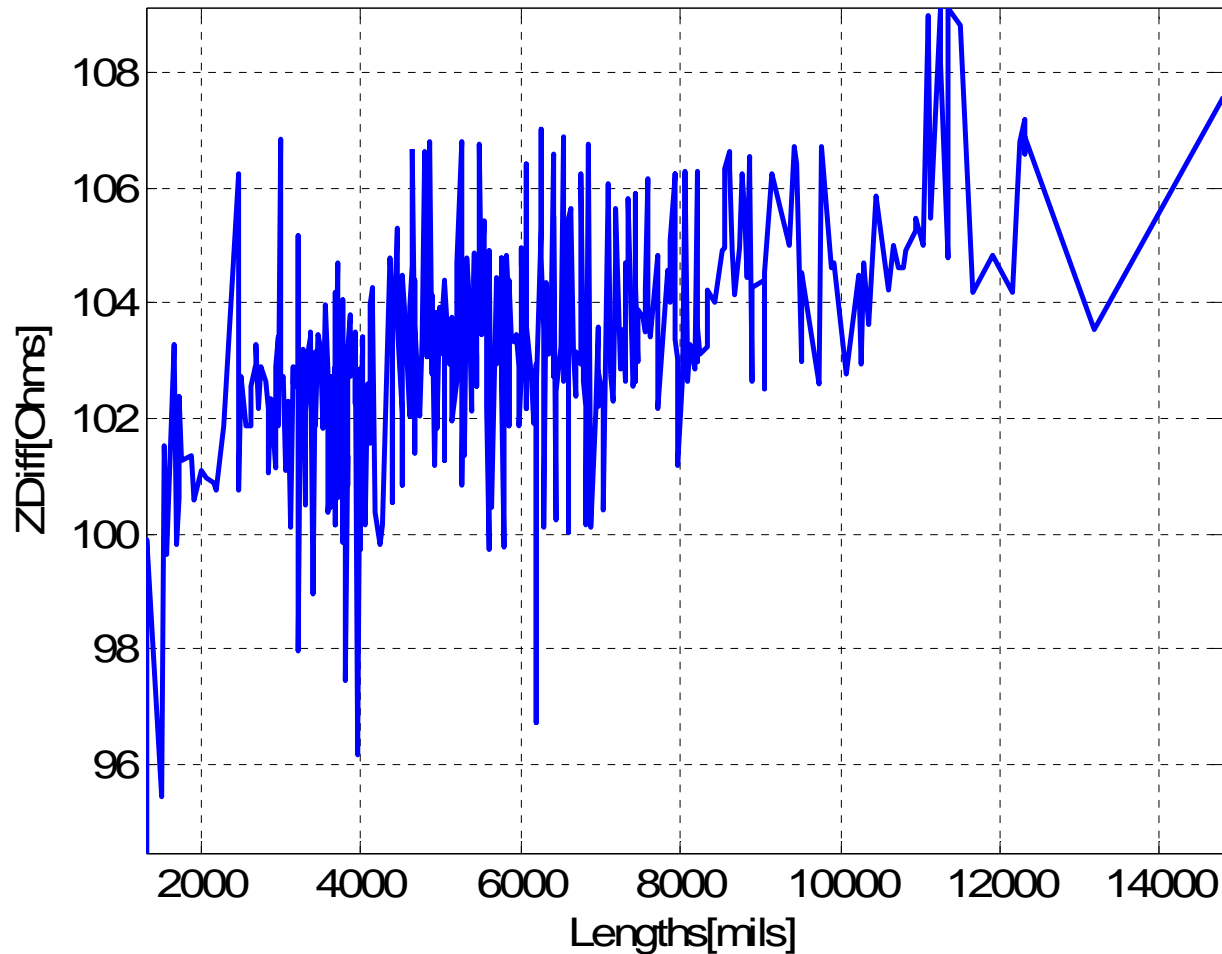
Plot shows measured  
average impedance  
over trace as a  
function of trace  
length

# Statistics Fab. B



- Consistent impedance  
Some outliers:
- Measurement errors
  - Extra vias on net

# Measured Differential Impedance vs. Trace Length (Fab. B)

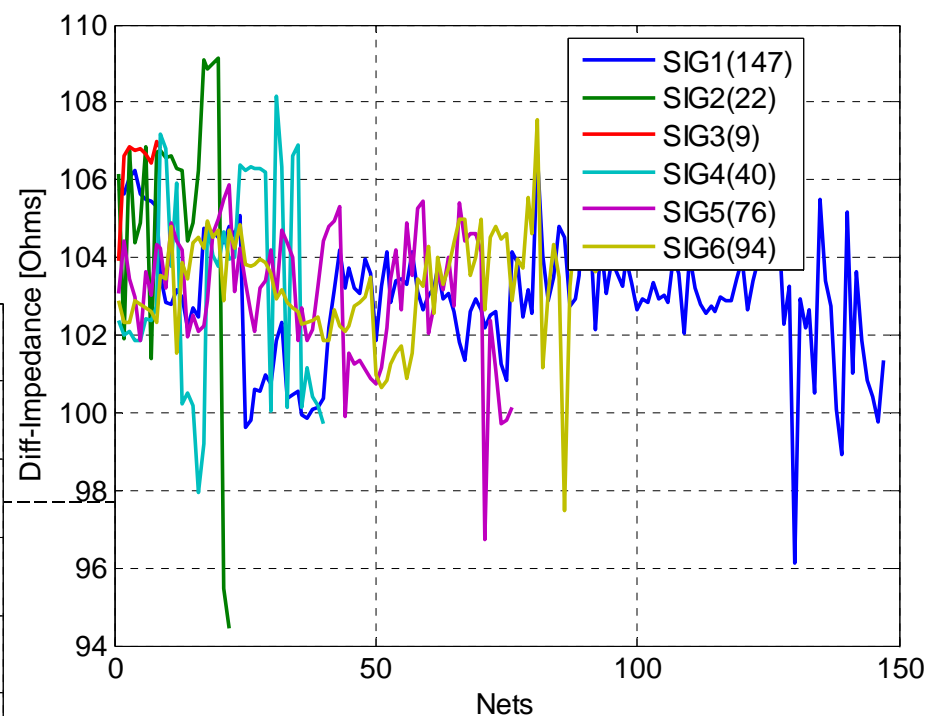
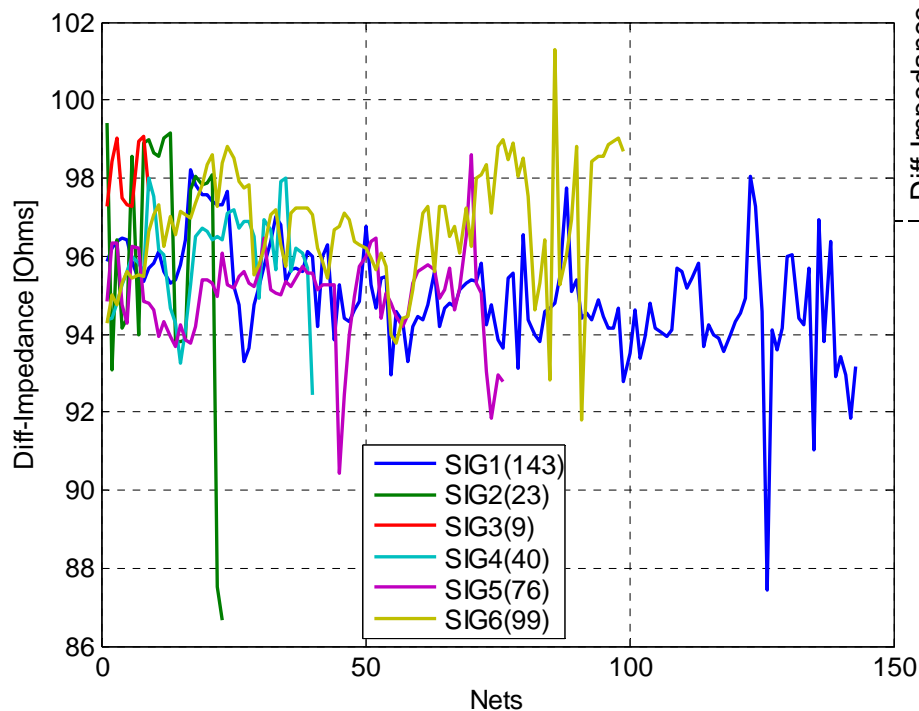


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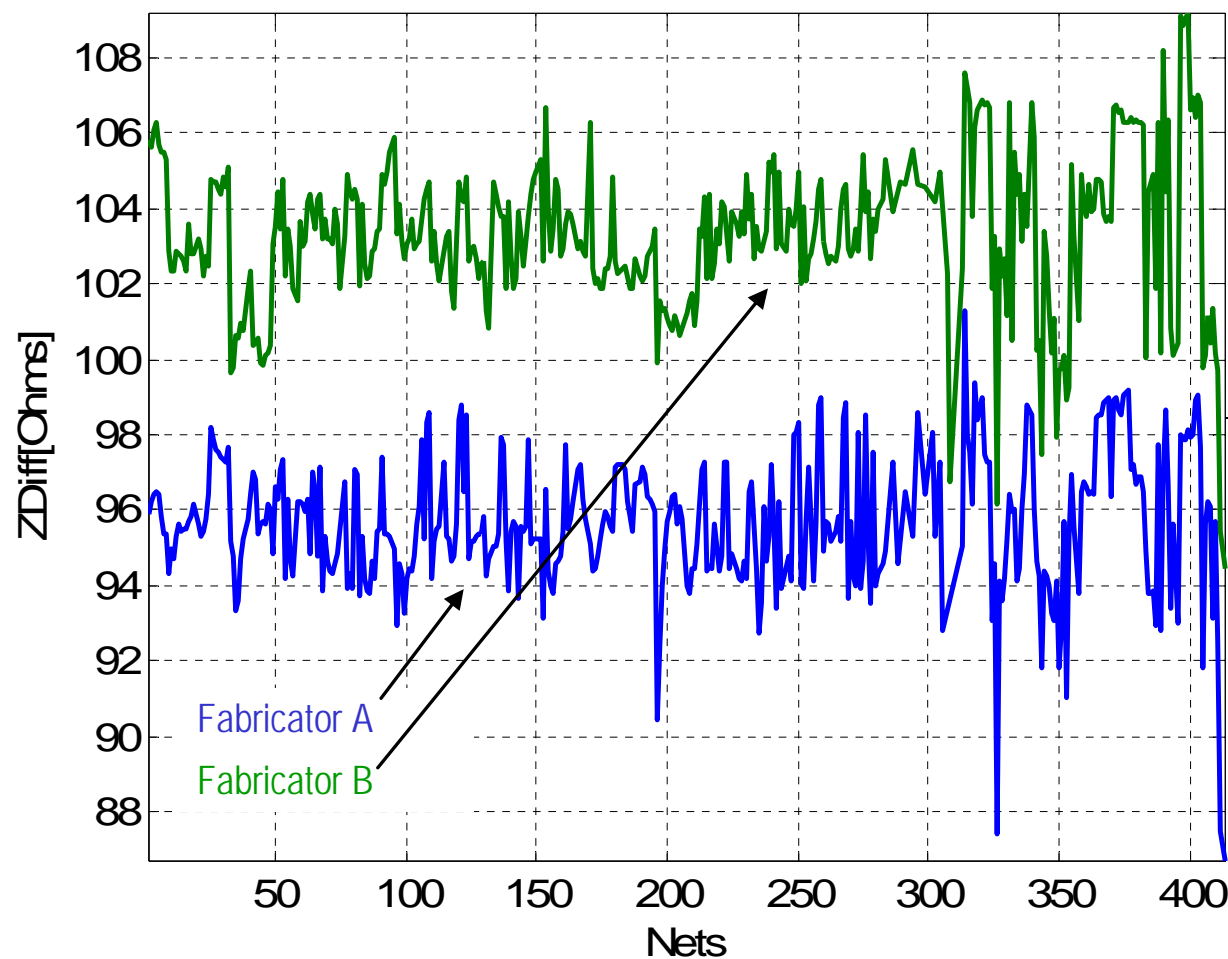
# Layer-to-layer Consistency

Fab. A



Fab. B

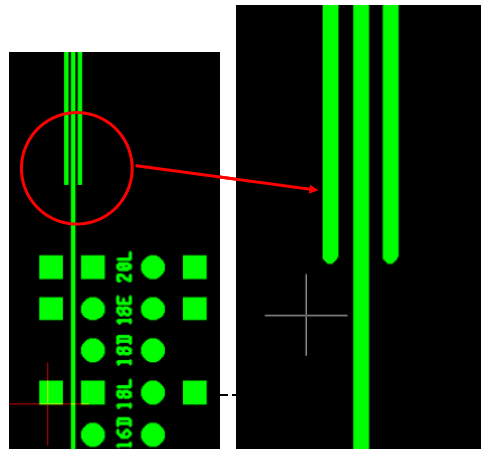
# Comparing Fab. A and Fab. B



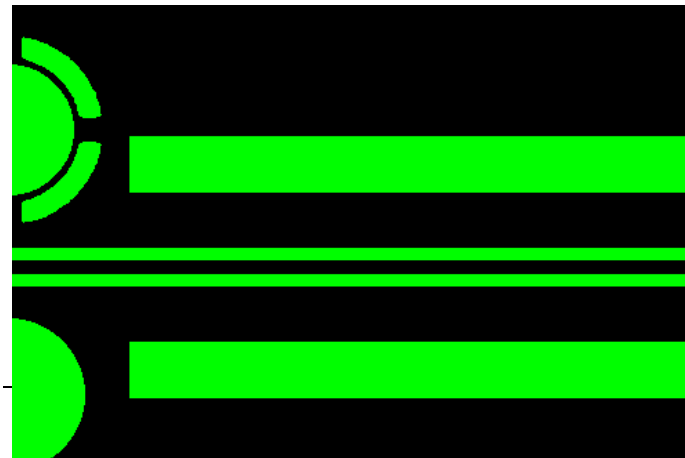
Consistent offset  
between the fabs  
Impedances of similar  
nets track well

# Comparing Test Coupons

Fab. A



Fab. B



There was no test coupon built into the board  
The test coupon was added by the fabricators

# Conclusions

After removing the outliers from the measured data, the impedance spread from layer to layer as well as over the entire board was around  $\pm 5$  ohms on the 100-ohm differential traces.

The average values, however, showed a systematic eight ohms difference between the two fabricators, which was not explainable by comparing the First Article Reports from the two fabricators.

The impedance offset was due to the differences in the impedance coupons used by the two fabricators.



THANK YOU

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